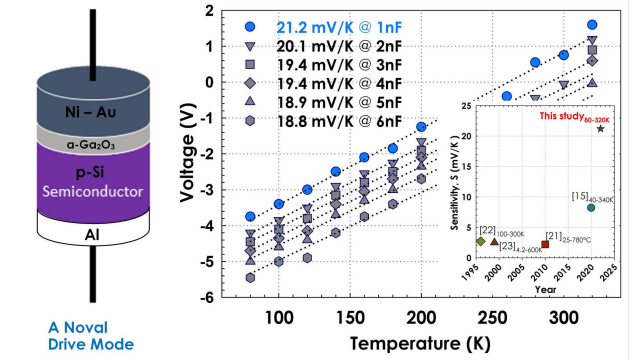
21.2 mV/K High-Performance $Ni_{(50\ nm)}$-$Au_{(100\ nm)}/Ga_2O_3/p$-Si Vertical MOS Type Diode and the Temperature Sensing Characteristics With a Novel Drive Mode

Osman Çiçek, Engin Arslan, Şemsettin Altındal, Yosef Badali, and Ekmel Özbay

***Abstract*—Sensitivity (*S*) and drive mode are crucial issues for the vertical metal-oxide-semiconductor (MOS) type diode applied in temperature sensing. In this study, experimentally, we indicated that the *S* values of the $Ni_{(50\ nm)}$-$Au_{(100\ nm)}/Ga_2O_3/p$-Si vertical MOS type diode, using the measured capacitance–voltage (C_m–V) outputs, are obtained with a novel drive mode. We applied the constant capacitance mode to drive the silicon thermo-diodes as well as constant current mode, and constant voltage mode, which are known as two different methods in the literature. Meanwhile, the *S* value is 21.2 mV/K at 1 nF. This value is the highest value proven in the literature excepting the cryogenic temperature region, and near room temperature. This study provided an original structure for the silicon thermo-diodes and a novel way to drive them.**



***Index Terms*—Novel drive mode, sensitivity, temperature sensing, vertical metal-oxide-semiconductor (MOS) type diode.**

I. Introduction

THE need for high-precision control in high-tech autonomous systems has led researchers to seek to produce advanced sensor devices that involve a wide thermal variation and a large temperature range for detection [1]. Integrated circuit (IC) temperature sensors, which are categorized into three major types: metal-oxide-semiconductor (MOS) based [2], bipolar junction transistor (BJT) based, and (polysilicon) resistor-based types, are preferred to improve the performances of conventional sensing solutions [1], [3]. To compensate for the requirements, MOS-type devices have gained great interest. Especially, vertical MOS-type devices have become the most useful temperature sensors [4].

Experimentally, Schottky and ohmic contacts are overlapped, so the electric field is both vertical and stronger rather than transverse due to the distance between the contacts. In this case, in the MOS type structures, using a thin interfacial layer between metal and semiconductor, can easily prevent an interface diffusion and reaction between metal and semiconductor and so, deactivates many surface states.

Temperature sensing by a vertical MOS-type device can be done by measuring the saturation current of the device [5], [6]. In addition, the temperature coefficient of the MOS-type diode is described as a maximum change in the measured capacitance (C_m) values in a specified temperature range. In the temperature-dependent measured capacitance–voltage (C_m–V) outputs of the MOS-type structures, the C_m values increased in the depletion region as the temperature increased. The C_m–V outputs with temperature, frequency, and the bias voltage applied are the results of the existence of surface states/traps, barrier-inhomogeneities, polarization, and series-resistance (R_s). Surface states are usually effective in the depletion region and weak inversion regions, but the interfacial

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layer and R_s are effective only in the accumulation region and the bias voltage applied will be shared between R_s, interface states, and depletion layer [7], [8]. With this approach, there is a change in the C_m values with respect to temperature with confirmed reordering and restructuring of charges in the interface of the device [9].

In terms of thermal improvements, to be an alternative to reduce the need for expensive and bulky cooling systems, switching devices made of wide bandgap semiconductors such as Ga_2O_3 have higher efficiency and thermal tolerance compared to Si [10], [11], [12], [13]. On the other hand, although Ga_2O_3 has low thermal conductivity, heat transfer is achieved by growing on a different heat sink substrate or by mono or bilayer top-side contact [13], [14]. Therefore, stability in power conversion systems depends on thermally stable Schottky or rectifier contacts. Fares et al. [13] reported the thermal stability of the W-based and the conventional Ni/Au contacts on β-Ga_2O_3.

In this study, we propose a significantly improved $Ni_{(50\ nm)}$-$Au_{(100\ nm)}/Ga_2O_3/p$-Si vertical MOS type diode to respond to a sudden change in temperature. This study provided the constant capacitance mode to drive the silicon thermo-diodes, as a novel method for temperature sensing.

II. Device Structure and Fabrication

Triethylgallium (TEG) ($(C_2H_5)_3Ga$) precursors and O_2 plasma as precursors were used to deposit the amorphous Ga_2O_3 thin film on 10 × 10 mm^2 dimensions p-Si substrates by utilizing (plasma-enhanced atomic layer deposition) PEALD technology (Okyay ALD). Firstly, the temperatures of the reactor and vacuum line were adjusted to 240 °C and 200 °C, respectively. The remote O_2 plasma was created using an RF coil with an alternate RF power of 250 W. Each ALD cycle had four stages: 1) TEG pulse; 2) Ar purge; 3) O_2 plasma; and 4) Ar purge. The thin film was deposited at a pressure of 5 × 10^{-4} bar and a temperature of 250 °C. Following these steps, a nominally 30-nm thick Ga_2O_3 film was formed on a p-Si substrate, which was confirmed by a spectroscopic ellipsometer (Jobin Yvon-Horiba).

A 300-nm aluminum (Al) ohmic contact was coated on the back side of the p-Si substrate prior to the growing procedure. Rapid thermal annealing (RTA) equipment was used to anneal samples at 480 °C for 10 min in an N_2 environment. A Schottky contact, which has a circular area of 1 mm diameter, was formed on the a-Ga_2O_3 thin film surface after the growing process [see Fig. 1(a)]. A Schottky contact consists of Nickel (Ni-50 nm) and Gold (Au-100 nm) films.

To verify the surface quality of the a-Ga_2O_3 thin film produced on the p-Si substrate, the surface morphology was studied using atomic force microscopy (AFM) imaging over a 3 × 3 mm^2 scan size. The a-Ga_2O_3 exhibits a crack-free, mirror-like surface form as well as a smooth surface morphology with low roughness (rms = 0.78 nm) and low defect density, as shown in Fig. 1(b). To prove that the a-Ga_2O_3 thin film is amorphous, the grazing incidence X-ray diffraction (GIXRD) must be described. The GIXRD results are shown in Fig. 1(c). There was no discernible peak, indicating that the film is amorphous.

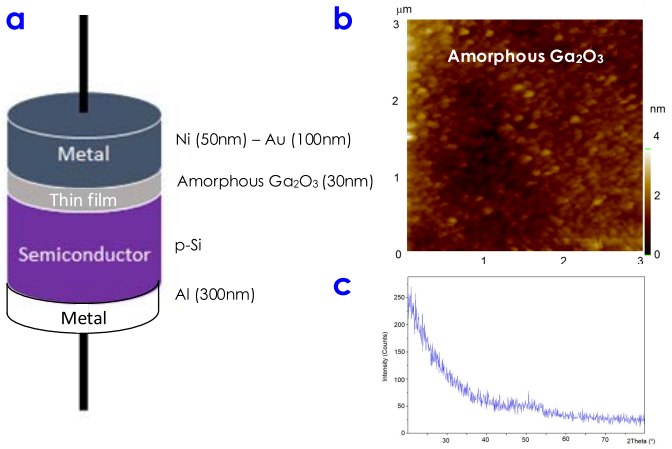

Fig. 1. (a) Schematic view of the $Ni_{(50\ nm)}$-$Au_{(100\ nm)}/Ga_2O_3/p$-Si Vertical MOS type diode. (b) AFM image of the surface with imaging over a 3 × 3 mm^2 scan size. (c) GIXRD measurement results for the a-Ga_2O_3 thin film.

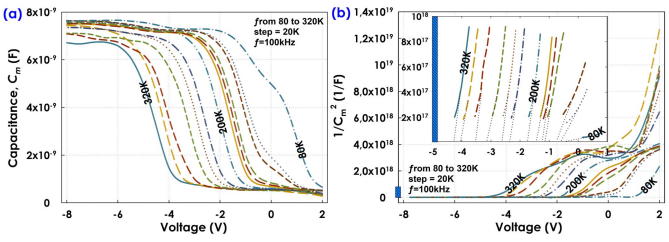

Fig. 2. (a) Temperature-dependent C_m–V characteristics of the $Ni_{(50\ nm)}$-$Au_{(100\ nm)}/Ga_2O_3/p$-Si vertical MOS type diode, measured in temperature range from 80 to 320 K at 100 kHz. (b) $1/C^2$ versus the bias voltage plots of a diode.

III. Results and Discussion

A. Main Characteristics

The electrical properties of the vertical MOS-type diode are examined as a function of temperature. To analyze the temperature sensing properties of $Ni_{(50\ nm)}$-$Au_{(100\ nm)}/Ga_2O_3/p$-Si vertical MOS-type diode with a novel approach, C_m–V measurements were carried out in the temperature range of 80–320 K at a frequency value of 100 KHz. The C_m–V–T measurement results are shown in Fig. 2(a). It can be clearly seen in the figure that the dispersion in the C_m–V curve is quite high for each temperature in the accumulation and depletion regions. In addition, the measurement results show that the capacitance characteristics of the vertical MOS diode are quite sensitive to the applied bias voltage and temperature of the sample. On the other hand, the C_m–V curve of the MOS structure has peaks in the accumulation region for all temperature values. This behavior can be attributed to the reordering of charges at the trap center with the effect of temperature and applied potential [7]. Herein, the high-dielectric interlayer used is important to increase the capacitance ($C_m = \varepsilon'(\varepsilon_o A/d)$) or store more charges/energy. Similarly, the ideality factor ($n = 1 + d/\varepsilon_{ox}\ (\varepsilon_s/W_D + qN_{ss})$ may be approximated to the ideal case ($n = 1$) by using high-dielectric interfacial layer instead of standard or conventional insulators like SiO_2 or SnO_2 and hence decrease of interfacial traps (N_{ss}).

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TABLE I
CALCULATED ELECTRONIC PARAMETERS OF THE $Ni_{(50\ nm)}$-$Au_{(100\ nm)}$/Ga_2O_3/p-Si VERTICAL MOS TYPE DIODE

T (K)	N_a (cm^{-3}) $x10^{17}$	E_F (eV)	V_{bi} (V)	$\phi_{Bo(C_m-V)}$ (eV)	$\Delta\phi_B$ (eV)	W_D (nm)	E_m (V/cm) $x10^5$	R_s (Ω) *at -8V*
80	1.35	0.081	4.213	4.229	0.072	201.1	4.19	92.0
100	1.27	0.090	4.014	4.047	0.066	202.2	3.97	87.4
120	1.35	0.096	3.480	3.521	0.065	182.8	3.81	91.7
140	1.30	0.102	3.188	3.239	0.063	178.1	3.58	93.0
160	1.29	0.108	2.689	2.751	0.060	164.4	3.27	91.9
180	1.26	0.113	2.384	2.454	0.058	156.6	3.04	92.7
200	1.21	0.118	1.793	1.875	0.053	138.6	2.59	91.5
220	1.25	0.120	1.400	1.489	0.051	120.6	2.32	93.9
240	1.37	0.121	1.293	1.384	0.051	110.4	2.34	94.1
260	1.40	0.124	1.186	1.282	0.050	104.7	2.27	93.9
280	1.30	0.128	0.907	1.014	0.046	95.0	1.91	94.2
300	1.20	0.133	0.776	0.892	0.043	91.5	1.70	96.4
320	1.11	0.137	0.629	0.754	0.040	85.7	1.47	96.2

The temperature-dependent electrical parameters of the $Ni_{(50\ nm)}$-$Au_{(100\ nm)}$/Ga_2O_3/p-Si vertical MOS type diode were obtained from the C_m^{-2}–V–T data. The C_m^{-2}–V data at various temperatures are shown in Fig. 2(b), in which we observe a linear dependence of C_m^{-2} on applied voltage (V) in the temperature range of 80–320 K. To see the behavior better, a part of the graph was focused on the relevant region and is shown in the inset of Fig. 2(b). It is observed that the voltage dependence of the C_m^{-2} has a linear behavior and almost all the curves are parallel to each other in the temperature range of 140–320 K. The built-in voltage (V_{bi}) value can be calculated from the C_m^{-2}–V graph by the extrapolation of the C_m^{-2} data to the bias voltage axis. The intersection voltage value of the voltage axis is the V_{bi} [8].

As can be seen from Table I, the V_{bi} values vary widely in the range of nearly 0.63–4.21 V. The large intercept voltage is the result of the high-dielectric Ga_2O_3 interfacial layer. It is evident that the vertical MOS diode has a great sensitivity against temperature changes.

Additionally, the important electrical parameters of the $Ni_{(50\ nm)}$-$Au_{(100\ nm)}$/Ga_2O_3/p-Si vertical MOS type diode, such as diffusion potentials (V_D), the depletion region width (W_D), and the acceptor density (N_a) values, were calculated using the C_m^{-2}–V data in the temperature range of 80–320 K using the equations follows:

$$V_D = V_{bi} + \frac{kT}{q} \tag{1}$$

$$W_D = \sqrt{\left(\frac{2\varepsilon_S\varepsilon_0 V_D}{qN_a}\right)} \tag{2}$$

$$N_a = \frac{2}{(q\varepsilon_S\varepsilon_0 A^2 \tan x)}. \tag{3}$$

The W_D values change between 201.1 and 85.7 nm as a function of temperature (see Table I). As seen in (2), the W_D value is directly proportional to intercept voltage (V_{bi}) or V_D and inversely proportional to the concentration of acceptor atoms (N_a). However, the increase in C_m value with increasing temperature leads to a small intercept or diffusion potential in the C_m^{-2} versus V plots and so, N_a. Therefore, the W_D value decreases with increasing temperature for a constant frequency.

The fermi level (E_F) of the vertical MOS diode can be determined using the equation given in [8]. It should be noted that the effective density of states (N_C) and the effective mass of electrons (m_e^*/m_0) are equal to $4.28x10^{15}T^{3/2}(m_e^*/m_0)^{3/2}$ and 1.08, respectively. In addition, the barrier height ($\phi_{Bo(Cm-V)}$) is expressed by equation $\phi_{Bo(C-V)} = V_D + E_F - \Delta\phi_B$. Herein, the $\Delta\phi_B$ is the lowering of the image force barrier, which is calculated using the equation given in [8]. Furthermore, the electric field (E_m) values change between 4.19 × 10^5 and 1.47 × 10^5 V/cm as a function of temperature (see Table I).

Since the barrier height ($\phi_{Bo(Cm-V)}$) is not homogeneous and contains many patches or lower barriers at around mean barrier height, under forward bias and at lower temperatures, many carriers with low energies can easily pass through these lower barriers or patches, thus causing an increase in the current or ideality factor [9], [15]. Under the reverse bias, however, the $\phi_{Bo(Cm-V)}$ cannot effect by the inhomogeneities at low temperatures. Therefore, it can be said that the dominant conduction mechanism at room or above temperatures is almost standard thermionic emission (TE) theory. Additionally, it considerably deviates from the ideal case at lower temperatures. Because, the TE, tunneling [thermionic field emission (TFE) and field emission (FE)], and tunneling via surface states may play roles either alone or collectively. Therefore, the measuring or the calibration of the capacitance signal for the accuracy and reliability of the temperature sensor can be applied at a sufficiently high frequency according to the current voltage. However, the surface states, polarization, and noise become more effective in the impedance measurements, at low frequencies.

The variation of $\phi_{Bo(Cm-V)}$ values with temperature was calculated and given in Table I for the $Ni_{(50\ nm)}$-$Au_{(100\ nm)}$/Ga_2O_3/p-Si vertical MOS type diode. The $\phi_{Bo(Cm-V)}$ values change between 4.229 and 0.754 eV. Herein, especially, the higher value of surface states at low temperatures and the existence of an interfacial insulator layer (Ga_2O_3) leads to a large intercept in the C_m^{-2} versus V plots and so, barrier height ($\phi_{Bo(Cm-V)} = V_{bi} + kT/q + E_F$). In addition, the apparent barrier height at low temperatures is considerably higher than at high temperatures because the value of forbidden bandgap energy or barrier height decreases with increasing temperature, and also the electronic charges gain more energy to pass over barrier height. Additionally, we have observed a drastic change in $\phi_{Bo(Cm-V)}$ values with respect to temperature change. This behavior is more evidence of the vertical MOS-type diode demonstrating great sensitivity against temperature changes.

The equivalent admittance based on measured capacitance (C_m) and measured conductance (G_m/ω), as shown in Fig. 3(a), was estimated by Nicollian and Brews as $Y = G_m + j\omega C_m$, whereas it is considered as a function of the applied frequency [7].

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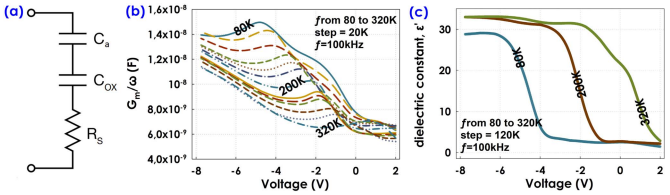

Fig. 3. (a) Electrical equivalent circuit with C_m and G_m in a variety of different circuit configurations. (b) G_m/ω-V-T characteristics of the $Ni_{(50\ nm)}$-$Au_{(100\ nm)}/Ga_2O_3/p$-Si vertical MOS type diode. (c) Calculated ε'-V-T data with responding to a sudden change in temperature range from 80 to 320 K at 100 kHz.

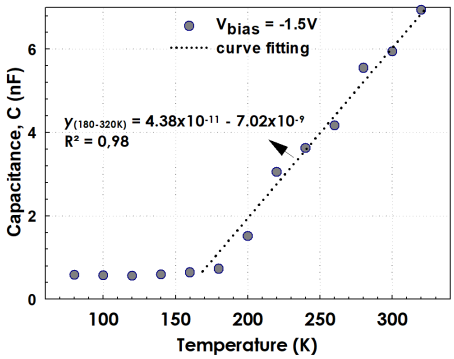

Fig. 4. Temperature-dependent C values of the vertical MOS diode at a constant bias voltage value.

The G_m/ω outputs, which consist of the accumulation, depletion, and inversion regions, are plotted in Fig. 3(b). A gradual increase is observed toward the depletion region for G_m/ω values of the vertical MOS diode, and on the other hand, they tended to increase in the strong accumulation region as the temperature decreased.

The series resistance (R_s) can be calculated in the strong accumulation region from the G_m/ω-V-T curve, using the equation given in [7]. The R_s values were calculated under the bias voltage of -8 V as the temperature varied. The calculated R_s values change between 92.0 and 96.2 Ω (see Table I). The R_s value is very low, and its value is nearly constant in the measured temperature interval between 80 and 320 K at the same bias voltage. This is a desirable condition for temperature sensing.

Another important parameter is the dielectric constant (ε') of the MOS-type diodes. The generalized equation between the C_m, the ε', and the capacitance value (C_o) of an empty capacitor is expressed as $\varepsilon' = C_m/C_o$. Additionally, the generalized equation of the C_o is calculated using the $C_o = \varepsilon_0(A/d)$ equation. Here, A is a rectifier contact area and equals 7.854×10^{-3} cm^2. The layer thickness (d) is 30 nm for the diode. The calculated ε' values vary in the range of nearly 1.42 to 33 depending on the bias voltage [see Fig. 3(c)]. In addition, very high dispersion was obtained in the ε'-V curve at the varied temperature values. The ε' value, which equals 33 at -8 V for 200 and 320 K, is almost nine times higher than the maximum value of traditional SiO_2.

B. Sensor Characteristics and a Novel Drive Mode

There are many more techniques used for sensing temperature that utilize diverse physical phenomena such as radiation, thermoelectricity, thermal expansion, etc. One of these techniques is selected in line with special requirements and constraints.

Diodes can be used in temperature measurement because the current passing through the diodes changes too much with the temperature in the forward bias voltage. Many different semiconductor material-based diode structures, such as silicon, germanium, and selenium, have been reported in the literature as temperature sensors.

The constant current mode, and constant voltage mode, which are known as two different methods in the literature, are widely used to drive the silicon thermo-diodes [16].

The constant current mode, which is the most preferred drive mode, is operated at a constant forward current, and the voltage drop across the diode is almost a linear function of the absolute temperature in a wide temperature range [16]. In constant voltage mode, which is another driving mode, the change of the current depending on the temperature is measured at constant voltage values and the diode is calibrated [17]. In this mode, the thermodiode can operate to measure temperature either in forward bias or reverse bias.

In this study, temperature-dependent capacitance measurements were done at constant bias voltage values in the silicon thermodiodes. From the measurement results, it was determined that the capacitance change due to temperature was quite high. Temperature sensing capability, which is very important in temperature measuring devices, is explained by the linear variation of the measured parameter with temperature. The temperature coefficient of an MOS-type diode is usually described as a maximum change in the C_m values in a specified temperature range. Therefore, the variation of the C_m value of the vertical MOS diode with temperature is obtained and shown in Fig. 4. Linear behavior is observed in a wide temperature range in the C_m–T graph. The C_m value increases linearly over a temperature range of 180–320 K at -1.5 V. However, it is almost constant at a low-temperature range between 80 and 160 K. The change in the C_m value with respect to temperature was calculated as 43.9 pF/K at -1.5 V, $R^2 = 99\%$ (see Fig. 4). These results show that a temperature sensor can be developed using temperature-dependent capacitance measurements at a constant voltage value.

In addition, the variation of voltage with temperature was obtained at a constant capacitance value and shown in Fig. 5(a). As seen in Fig. 5(a), the voltage drop is almost a linear function in a wide temperature range with a voltage change at a constant capacitance value. Theoretically, when increasing the temperature, the free electron charges gain more energy to overcome the barrier height. As in [18], [19], and [20], the temperature response depends on various parameters such as voltage or electric stress, the study frequency, polarization, interface states, and their relaxation/life-time. In our study, there is a relationship between sensitivity and temperature for the capacitance as $C(T) = C_{o(0\,K)} + \alpha T$, and α is

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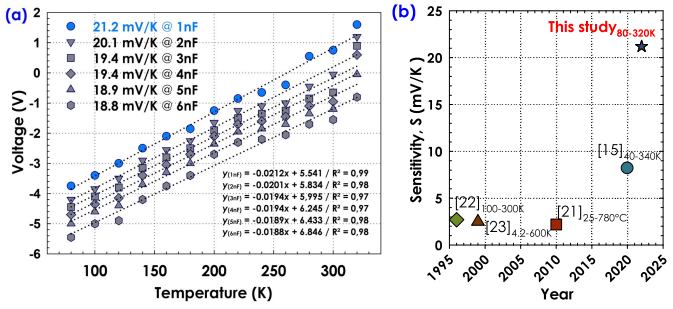

Fig. 5. (a) Bias voltage versus temperature plots at constant capacitance values. The highest S values were given in the graph. (b) Highest S values were given, which are, as in mV/K, obtained from constant voltage and constant capacitance mode, excepting the cryogenic temperature region, and near the room temperature.

TABLE II

COMPARISON OF THE $Ni_{(50\ nm)}$-$Au_{(100\ nm)}$/Ga_2O_3/p-Si VERTICAL MOS TYPE DIODE AND SILICON/SILICON ON INSULATOR (SOI)-BASED DEVICES

Structure	Temperature range	Sensitivity, S	Diode drive mode	Ref.
graphene-PVP/n-Si	40 to 340 K	−1.30 to −8.2 mV/K from 0.1 μA to 10 μA @ LTs −1.93 to −7.9 mV/K from 0.1 μA to 10 μA @ HTs 7.24 to 6.9 mA/K from 1.5 V to −1.5 V @ LTs 22.9 to 33.2 mA/K from 1.5 V to −1.5 V @ HTs	Constant current Constant voltage	[15]
SOI CMOS	25 to 780 °C	−2.2 mV/K for 14 nA −1.3 mV/K for 65 μA	Constant current	[21]
Cryogenic Si Diode	10 to 100 K*	−15. 1 to −21.8 mV/K from 0.1 A to 100 μA	Constant current	[22]
	100 to 300 K	−1.41 to −2.7 mV/K from 0.1 A to 100 μA		
Silicon	4.2 to 600 K	< 2.5 mV/K from 0.1 μA to 100 μA	Constant current	[23]
Cryogenic Temperature Sensor – Si Diode ®	1.4 K* 4.2 K* 10 K* 77 K* 305 K	-12.5 mV/K for 1.64 V - 31.6 mV/K for 1.58 V -26.8 mV/K for 1.38 V -1.73 mV/K for 1.03 V -2.30 mV/K for 0.56 V	Constant voltage	[24]
Ga_2O_3/p-Si	**80 to 320 K**	**−21.2 to −18.8 mV/K from 1 nF to 6 nF**	**Constant capacitance**	**This study**

* Cryogenic temperature region (0 K to 123 K)
® Industrial diode

the temperature coefficient of capacitance for a constant bias voltage, but as can be seen in Fig. 5(a), its value changes with applied bias voltage. This result gives us the opportunity to develop a newly derived mode, which we can call the constant capacitance mode.

The constant capacitance mode can be considered a novel driving mode. In constant capacitance mode, temperature-dependent voltage values are read at the same capacitance value, and sensitivity (S) is defined as mV/K. A high S value was obtained for the $Ni_{(50\ nm)}$-$Au_{(100\ nm)}$/Ga_2O_3/p-Si vertical MOS type diode in the constant capacitance mode. This result shows that it is possible to make precise measurements with the aforementioned mode in the high-temperature range.

For all the devices, R^2 is over 97%, confirming the relevance of the results. Moreover, the S value is 21.2 mV/K at 1 nF, $R^2 = 99\%$ [see Fig. 5(a)]. When comparing this with the literature, the S value at 1 nF is the highest value as proven in the literature, excepting the cryogenic temperature region, and near the room temperature [see Table II and Fig. 5(b)]. Moreover, it demonstrates very high sensitivity in MOS-based temperature sensors.

IV. CONCLUSION

In this study, we have obtained the higher S values in the $Ni_{(50\ nm)}$-$Au_{(100\ nm)}$/Ga_2O_3/p-Si vertical MOS-type diode using the C_m–V characteristics. We applied the constant capacitance mode to drive the silicon thermo-diodes as well as two different methods known in the literature. This study provided an original structure for the silicon thermo-diodes and a novel way to drive them. The 21.2 mV/K sensitivity at 1-nF capacitance was measured between 80 and 320 K temperature in the $Ni_{(50\ nm)}$-$Au_{(100\ nm)}$/Ga_2O_3/p-Si vertical MOS type diode. This value is the highest value that is proven in the literature, excepting the cryogenic temperature region, and near the room temperature. We concluded that the vertical MOS diode with its high sensing ability is a good candidate for its use in thermal sensors in a wide temperature range.

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